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10/808,305	03/25/2004	Yuichi Gomi	042262	5494

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EXAMINER	
WANG, KENT F	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,305	GOMI, YUICHI	
	Examiner	Art Unit	
	KENT WANG	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendments, filed on 01/04/2008, have been entered and made of record. Claims 1-9 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 2, 4, and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Juen (US 6,542,194) in view of Krymski (US 6,809,766).

Regarding claim 1, Juen discloses a XY-addressing type solid-state imaging apparatus (imaging element 45 is an XY address type imaging element) comprising:

- a plurality of pixels arranged in a two-dimensional matrix (the imaging element in Fig 8 has a plurality of pixels disposed in matrix) (7: 18-29); and
- a horizontal scanning circuit (a horizontal scanning circuit HSR65, Fig 8) and a vertical scanning circuit (a vertical scanning circuit VSR61, Fig 8) for reading signals of the pixels (10: 11-20);

Juen discloses a vertical scanning circuit (VSR61) in a pixel reset period selects the pixels at a first timing to concurrently effect only a reset operation of the pixels thereof and selects at a second timing subsequent to the first timing the pixels of the address different from the rows selected at the first timing to concurrently effect only a reset operation of the pixels (the start time point of the reset scanning of the imaging element 45, step S6 in Fig 5; the reading scanning is performed and the read image signal can begin to be recorded to the signal recorder 50 through the signal processor 48, step S10, Fig 5) (8: 10-37, Juen) thereof, reset operation in this manner being repeated to effect a reset operation of all pixels (reset scanning position 3 move from the top to the bottom of the imaging surface 5 at a specified interval and this manner being repeated) (5: 48-63, Juen).

Juen does not disclose a sensor in a pixel reset period concurrently selects the pixels of n rows at a first timing to concurrently effect only a reset operation of the pixels of the n rows thereof and selects at a second timing subsequent to the first timing the pixels of n rows of the address different from the rows selected at the first timing to concurrently effect only a reset operation of the pixels of the n rows.

Krymski discloses a sensor in a pixel reset period concurrently selects the pixels of n rows at a first timing (shown at 600 in the flowchart of Fig 6, the shutter pointer 1 is set to the desired width and Fig 7 shows the system operating with the current shutter width of three rows) to concurrently effect only a reset operation of the pixels of the n rows thereof and selects at a second timing subsequent to the first timing the pixels of n rows of the address different from the rows selected at the first timing to concurrently effect only a reset operation of the pixels of the n rows (when the read pointer reaches the top, as detected at

604, the shutter pointer 2 is set to the new width and when the shutter pointer 2 reaches the end of the frame, as detected at 608 and shown in Figs 11 and 12, it is enabled to initiate the new shutter width and the read pointer 200 is still reading three rows behind the shutter pointer 300) (4: 1-34, Krymski).

Thus it would have been obvious to a person of the ordinary skill in the art at the time of the invention to modify Juen's image apparatus to use the rolling shutter as taught by Krymski, as to sequentially reset rows of the pixel array without generating any flashes when the exposure time is increased, thus circumvents the need for address calculations (2: 19-24 and 4: 35-43, Krymski).

Regarding claim 2, Krymski discloses the pixels of the n rows concurrently selected for the reset operation to be effected are the pixels of the rows having consecutive addresses (Fig 7 shows the system operating with the current shutter width are on three adjacent rows) (4: 1-34, Krymski).

Regarding claim 4, Juen discloses the vertical scanning circuit comprises: a row selecting section (a vertical scanning circuit VSR61, Fig 8) (10: 11-20); and a timing pulse generating section (pulse generator 46, Fig 4) to which output signals of the row selecting section (VSR 61) and timing signals (scanning clock) are inputted to generate control signals for effecting pixel operation (the pulse generator 46 provides a clock signal to a signal processor 48, Fig 4) (7:18-29).

Regarding claim 6, Juen discloses a row selecting section comprises a shift register (a signal reading scanning register 62, Fig 8) (10: 50-57).

5. Claims 3, 7, and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Juen (US 6,542,194) in view of Krymski (US 6,809,766), and further in view of Suzuki (US 6,975,357).

Regarding claim 3, Juen and Krymski do not disclose the pixels of the n rows concurrently selected for the reset operation to be effected are the pixels of the rows having discrete addresses. However, Suzuki discloses the pixels of the n rows concurrently selected for the reset operation to be effected are the pixels of the rows having discrete addresses (first vertical scan circuit 30 is put in charge of odd-number rows and the second vertical scan circuit 31 is put in charge of even number rows, Fig 11) (9: 50-67 and Fig 11).

Thus it would have been obvious to a person of the ordinary skill in the art at the time of the invention to modify Juen and Krymski's image apparatus to use the sensor as taught by Suzuki, so as the information of all the pixels can be picked up in half a time at the same operating frequency, thereby implementing the high-speed image pickup operation (9: 60-67, Suzuki).

Regarding claim 7, the limitations of claims 1 and 4 are taught above, Suzuki discloses a timing pulse generating section (timing generator 32, Fig 1) comprises a logic circuit (AND gate 35*n*, Fig 1; 4: 48-54). Thus it would have been obvious to a person of the ordinary skill in the art at the time of the invention to choose the logic gate circuit as taught by Suzuki, as each output of the AND gates is supplied through the read-out line to the drain of the read-out selection transistor in each pixel which can eliminate the vertically-striped system noise in principle and prevent increase of the power consumption and deterioration of the SN ratio (2: 7-14 and 4: 48-54, Suzuki).

Regarding claim 9, this claim recites same limitations as claim 7. Thus it is analyzed and rejected as previously discussed with respect to claim 7 above.

6. Claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Juen in view of Krymski, and further in view of Kochi (US 6,947,088).

Regarding claim 5, Juen and Krymski disclose a solid-state imaging apparatus comprising a vertical scanning circuit. Juen and Krymski do not explicitly disclose the vertical scanning circuit comprises a decoder.

Kochi discloses a vertical scanning circuit comprises a decoder circuit (5: 49-51, Kochi). Juen, Krymski and Kochi are analogous art because they are from the same field of endeavor of a XY-addressing type solid-state imaging sensor for an image pickup device. At the time of the invention, it would have been obvious to a person of the ordinary skill in the art to use Kochi's encoder circuit in Juen and Krymski's solid-state imaging device. The suggestion/motivation would have been to enable the vertical scanning circuit to freely select the pixel column selection order, thereby can realize various signal read-out orders in comparison with the shift register circuit (5: 50-56, Kochi).

7. Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Juen in view of Krymski and Kochi, and further in view of Suzuki (US 6,975,357).

Regarding claim 8, the limitations of claims 1, 4, and 5 are taught above, Suzuki discloses a timing pulse generating section (timing generator 32, Fig 1) comprises a logic circuit (AND gate 35*n*, Fig 1; 4: 48-54). Thus it would have been obvious to a person of the ordinary skill in the art at the time of the invention to choose the logic gate circuit as taught by Suzuki, as each output of the AND gates is supplied through the read-out line to the drain

of the read-out selection transistor in each pixel which can eliminate the vertically-striped system noise in principle and prevent increase of the power consumption and deterioration of the SN ratio (2: 7-14 and 4: 48-54, Suzuki).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Hynecek (US 7,079,178), Hashimoto (US 2003/0025815), Kaplinsky et al (US 7,142,234), Van Blerkom (US 7,084,914), Yadid-Pecht (US 6,831,689), and Kimura (US 7,218,349).

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kent Wang whose telephone number is 571-270-1703. The examiner can normally be reached on 8:00 A.M. - 5:30 PM (every other Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-270-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://portal.uspto.gov/external/portal/pair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free)? If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KW
19 June 2008

/Ngoc-Yen T. VU/
Supervisory Patent Examiner, Art Unit 2622